APPLICATION FOR
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IN THE NAME OF

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FOR

TIMING RECOVERY WITH VARIABLE BANDWIDTH PHASE LOCKED LOOP AND NON-LINEAR CONTROL PATHS

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TITLE OF THE INVENTION

TIMING RECOVERY WITH VARIABLE BANDWIDTH PHASE LOCKED LOOP AND NON-LINEAR CONTROL PATHS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to communications systems that handle a wide variation in data density, large amplitude jitter with a wide frequency range, and imperfect equalization, such as T1 networks. More particularly, the present invention relates to a timing recovery system including a linear phase-locked loop ("PLL") with a variable bandwidth loop filter and three proportional paths with non-linear control.

2. Discussion of the Related Art

Networking applications have become popular in recent years, in response to an explosion in the use and variety of networks employed in a vast array of computing settings. Correspondingly, many advances have been made in the related technology in order to improve the quality of these systems. For instance, fully integrated transceivers for T1 Channel Service Unit ("CSU") and Integrated Services Digital Network ("ISDN") Primary Rate Interface applications are known in the art, and are presently commercially available. These devices are useful for networking applications, such as timing recovery in T1 systems. However, there are obstacles that prevent such systems from providing good jitter tolerance, a desirable quality in communications networks, and other applications. Such obstacles can include exceptionally

large amplitude jitter, a wide variation in data density, large amounts of cable attenuation, and imperfect equalization.

Jitter is the general term used to describe distortion caused by variation of a signal from its reference timing position in a transmission communications system. In an ideal system, bits arrive at time increments that are integer multiples of a bit repetition time. In a real system, however, pulses arrive at times that deviate from these integer multiples. This deviation may cause errors in the transmission of data, particularly when data is transmitted at high speeds. The deviation or variation may be in the amplitude, time, frequency or phase of this data. Jitter may be caused by a number of phenomena, including inter-symbol interference, frequency differences between the transmitter and receiver clock, noise, and the non-ideal behavior of the receiver and transmitter clock generation circuits.

Jitter is a problem of particular import in digital communications systems for several reasons. First, jitter causes the received signal to be sampled at a non-optimal sampling point. This occurrence reduces the signal-to-noise ratio at the receiver and thus limits the information rate. Second, in practical systems, each receiver must extract its received sampling clock from the incoming data signal. Jitter makes this task significantly more difficult. Third, in long distance transmission systems, where multiple repeaters reside in the link, jitter accumulates.

Jitter amplitude is typically measured in unit intervals ("UI") where 1 UI equals 1 period of bit repetition time. For example, in T1 networks, 1 UI is equal to 648 microseconds and in E1 networks, 1 UI is equal to 488 microseconds. Normal ranges of jitter vary widely depending upon the specific application. For T1 systems, the incoming jitter is generally limited to approximately 5 UI peak-to-peak for jitter frequencies between 10 Hz and 40 KHz, and 0.1 UI peak-to-peak for jitter frequencies between 8 KHz and 40 KHz. However, T1 receivers

generally must be able to tolerate sinusoidal jitter with an amplitude as high as 0.4 UI between 10 KHz and 100 KHz, and as large as 28 UI at 300 Hz for network interoperability.

Accordingly, there is a need for a timing recovery system capable of providing improved jitter tolerance, especially for systems that must manage wide variations in data density and large amplitude jitter in large frequency ranges.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1a and 1b illustrate a block diagram of a digital phase locked loop with three non-linear proportional paths in accordance with an embodiment of the instant invention;

Fig. 2 illustrates a block diagram of a first non-linear proportional path in accordance with an embodiment of the instant invention;

Fig. 3 illustrates an eye diagram, depicting an operation of the non-linear proportional path of Fig. 2;

Fig. 4 illustrates a block diagram of a second non-linear proportional path in accordance with an embodiment of the instant invention;

Fig. 5 illustrates a flow chart of a machine-readable program code in accordance with an embodiment of the instant invention; and

Fig. 6 illustrates a receiver circuit in accordance with an embodiment of the instant invention.

DETAILED DESCRIPTION

In one embodiment of the present invention, a timing recovery system is provided. The system includes a PLL with a variable bandwidth loop filter, several data dependent gain units

and three proportional paths with non-linear control. The system provides improved jitter tolerance even with a wide variation in data density and large amplitude jitter over a wide frequency range. The gains of both an included loop filter and phase detector may be varied with both frequency and data density. Direct, unfiltered adjustments may be made to phase based on a received data pattern and phase error magnitude to reduce loop latency and provide a temporary and immediate boost in the loop gain of the PLL. Direct, unfiltered adjustments may also be made to phase based on the sign of the first differential of the accumulator output during long strings of zeros to help maintain tracking, even with a very low data density.

In another embodiment of the present invention, a method of providing enhanced jitter tolerance in a communications network is provided. A communications network with three non-linear paths and a PLL is provided. Data is input to the communications network. A phase error is estimated based on a data sample from both the center of the data eye of the input data and from a phase sample from the input data half-a-baud later in time. The phase error is then correlated with the sign of the recovered data. The correlated phase error is then multiplied by a gain. The multiplied and correlated phase error is filtered by a loop filter to generate an output. This output is summed with output from the non-linear paths to generate a summed output. Finally, the summed output is converted into clock phase information.

The system preferably implements a PLL, which may be of any suitable order. For instance, a second order PLL may be suitable for use in accordance with the various embodiments of the present invention. A PLL is a feedback control system designed to lock the phase of a local clock to the phase of an incoming signal. A PLL generally includes a phase detector whose output is proportional to the difference between the incoming phase and the output phase of an included voltage controlled oscillator ("VCO") or a digitally controlled

oscillator ("DCO"); a loop filter whose output is proportional to the input but with some desired frequency characteristic; and a VCO or DCO whose output phase is proportional to the integrated input voltage.

The components of a PLL may be implemented as either an analog or digital circuit. In operation, the phase detector computes the error (i.e., the difference between the incoming and local phase), which is then filtered by the loop filter and presented to the VCO, which changes its own output phase accordingly. Owing to overall negative feedback, the PLL tends to drive the error signal to zero, thus forcing the output phase of the VCO to be equal to the input phase.

The order of a PLL depends upon the number of integration operations included therein. The VCO or DCO provides one integration. Thus, a PLL with no integrators in the loop filter has an order of one. A second order PLL, which may be included in the embodiments of the present invention, includes one integrator in the loop filter.

A PLL can provide good jitter tolerance for many applications. However, some applications, such as timing recovery in T1 systems, require good jitter tolerance in the presence of exceptionally large amplitude jitter, which may range in frequency from 300 Hz to 100 KHz. Further, these systems must be capable of handling wide variations in data density, large amounts of cable attenuation, and imperfect equalization. This combination of impairments makes the design of the timing recovery PLL quite difficult. An additional impairment is found in systems based upon digital signal processor techniques where the latency between the sampling clock and the output of the timing recovery may be large.

For systems with such impairments, the performance of the timing recovery may be enhanced by adding several non-linear proportional paths, also referred to as gearshifts, to the PLL. The preferred timing recovery system **100** depicted in Fig. 1 contains three such paths, **1**, **2**

and **3**. The system includes a data density detector **4**, which monitors the received data density and adjusts the linear gain **102** and phase detector gain **9** to maintain a constant gain and bandwidth with variations in data density. The system also includes a frequency detector **5**, which detects the frequency of an incoming timing jitter and adjusts the bandwidth of the PLL to maximize the jitter tolerance over a wide range of frequencies.

The operation may be seen by reference to Fig. 3, which is an eye diagram. An eye diagram will be recognized by one skilled in the art as a method used to assess the signal-to-noise ratio of a random signal in a communications system. It is created by sampling the desired signal with a fixed clock (typically synchronized with the transmit clock) while transmitting random data and overlaying all of the received traces on top of one other. One can, by inspection, estimate the likelihood of making an error in the bit decision.

For example, as depicted in Fig. 3, when the timing recovery system of the present invention is operating correctly, the sampling point **304** is exactly in the center of the eye, and the distance between the decision threshold (+/- 0.5 V) and the signal is maximized. The first and second transitions **301** and **302**, respectively, that might trigger the first gearshift **1** are indicated along with the data sample with a positive phase error **305**, and the phase sample **306**. Assuming that the equalization of the receiver is designed to provide a reasonable pulse shape (i.e., one that is similar to a raised cosine pulse and thus possessing a minimum amplitude at integer multiples of the bit rate), then by judiciously selecting the threshold against which the data sample is compared, the amount of phase error necessary to trigger the gearshift may be selected. Preferably, the threshold for the first gearshift **1** in this system is approximately 0.27 V. The amount of phase adjustment provided by each correction is set by the gearshift 1 gain value.

Figs. 1a and 1b illustrate a block diagram of a preferred timing recovery system **100**. The core of this system is a digital PLL which may include a phase detector **6**, a proportional-plus-integral loop filter (**101**, **102**, **103**, **104**, **105**, **106**), and a digitally controlled oscillator **112**. The loop filter illustratively includes an accumulator (**104**, **105**, **106**) along with a linear gain **102**, an integrator path gain **103**, and a first summing node **101**. The accumulator may further include an integrator summing node **105**, a delay element **106**, and an integrator leakage element **104**. Herein, the digitally controlled oscillator **112** may be a digital to analog converter ("DAC") **112**.

The preferred timing recovery system **100** may further include gear shift 1 and 3 gain variables **15** and **12**, respectively; gear shift 1, 2, and 3 multipliers **16**, **18**, and **22**, respectively; gear shift 1 and 2 thresholds **13** and **14**, respectively; gear shift 3 gain element **21** and comparator **23**. Preferably, the system **100** also includes a phase error comparator **17**, a summing node **19**, a clock output **20**, a differentiator summing node **24**, a delay element **25**, and a summing node **26**.

In operation, the phase detector **6** preferably estimates the phase error based on two samples of the incoming signal: the data sample **7** from the center of the data eye and the phase sample **8**, half-a-baud later in time. The phase error may be correlated with the sign of the recovered data, multiplied by a gain **9**, and filtered by the loop filter at a first summing node **101**. The output of the linear filter may be summed with any outputs from the non-linear paths **1**, **2** and **3** at summing node **26** and converted into clock phase information by the DAC **112**. The gain and bandwidth of the linear PLL is preferably varied according to the received data density and the incoming jitter frequency. Each of the three non-linear paths **1**, **2** and **3** is preferably triggered by a different set of input conditions and is designed to boost the effective proportional path gain in that situation. The first gearshift **1** is preferably based on the received data pattern;

the second gearshift **2** is preferably based on the amplitude of the data samples; and the third gearshift **3** is preferably based on run-length or number of sequential zeros.

Fig. 2 shows a block diagram of a first gearshift **1**, which is a pattern-based operation. The circuit may receive phase sample **8**, data sample **7**, and data **10**, and look for strings of zeros followed by a plus or minus one. Preferably, absolute value functions **201** and **202**, and logical greater than functions **203** and **204** are included to assist in the location of this information. Most preferably, logical greater than function **203** returns an output of true where the absolute value of data sample **7** is greater than gear shift 1 threshold **13**. Similarly, logical greater than function **204** preferably returns an output of true where the absolute value of data sample **7** is greater than phase sample **8**. This data may then be multiplied through gear shift 1 multiplier **16** by a gear shift 1 gain **15** and output to summing block **19**. The first gearshift **1** illustratively depicted in Fig. 2 looks for strings of four zeros, owing to three delay elements (**205**, **206**, and **207**) being included therein. In alternate embodiments the first gearshift **1** may be designed to search for any appropriate number of zeros, by altering the number of delay elements.

The second gearshift **2**, shown in Fig. 4, is preferably triggered when the amplitude of the data sample **7** falls below a specified second gearshift threshold **14**, most preferably set at about 0.7 V, and the decision is a plus or minus one such as that indicated at sample point **303** in Fig. 3. This scenario may be presented when the data density is low (i.e., there is not much phase information) and the jitter amplitude is large. In such a situation, the PLL may not have enough phase information to properly track the incoming jitter, thus phase error can accumulate such that the data samples begin to approach the decision level. An immediate large step may therefore be made in the direction of the phase error. Although not depicted in Fig. 4, the size of the phase step may readily be varied by adding gain after the multiplier **18**.

The second gearshift **2** illustratively depicted in Fig. 4 may receive data sample **7**, data **10**, and phase detector output **405**. Preferably, absolute value functions **401** and **402**, and logical less than function **403** are included. Most preferably, logical less than function **403** returns an output of true where the absolute value of data sample **7** is less than gear shift 2 threshold **14**. Most preferably, the phase detector output **405** is manipulated through phase error comparator **17** and multiplied by multiplier **18** by the absolute value of data **10** ANDed with the logical less than function **403** output through gear shift 2, and output to summing block **19**.

The operation of a third non-linear path **3** may be seen in Figs. 1a and 1b. This third non-linear path, or gearshift **3**, is illustratively a counter that increments when the received data **10** is a zero and is reset when the data **10** is one. When the counter reaches the value set in the run length limit variable **11**, set at about 10 in a preferred embodiment, the output is preferably set high and an immediate step is made in the direction of the sign of the first differential of the accumulator output. This operation may help to reduce the accumulated phase error when there are long strings of zeros and the data density is low. In such a situation, there may be insufficient ones to provide enough phase error information to the loop filter, making it necessary to estimate the direction of the accumulated phase error. However, because of the relatively low bandwidth of the loop filter, the phase of the accumulator can lag the actual phase error by as much as 45 degrees. Thus, it is not necessarily the best estimate of the direction of the phase error. The first differential of the accumulator indicates the direction in which the phase error is changing and may be a better estimate for this condition.

Hold off counters (not shown) may further be included in the non-linear paths of the present invention. These counters prevent multiple triggers and the corresponding potential for over-adjustment. For example, if the third gearshift **3** has just triggered, it is possible that the

next input one could cause either the first gearshift **1** or second gearshift **2** to trigger as well, resulting in over-correction. The hold off counters prevent a single gearshift from triggering on sequential bits and prevent any gearshift from triggering within some number of bits of another.

In addition to the non-linear control paths, two other control elements are preferably included in the timing recovery system of the present invention. As shown in Figs. 1a and 1b, a data density detector **4** tracks the received ones density and adjusts the phase detector gain **9** and the linear gain **102** in order to minimize changes in the system response caused by variations in data density.

The frequency detector **5** may provide an estimate of the frequency of incoming jitter and may also be used to adjust PLL gains. The frequency detector **5** may further be utilized to adjust the accumulator leakage and gain to provide for greater rejection of high frequency jitter without sacrificing loop gain at lower frequencies.

The aforementioned embodiments of the instant invention may be embodied in a machine-readable program code, which may be further stored on a machine-readable storage medium. A most preferred embodiment of this code is illustratively depicted in flow chart form in Fig. 5. This most preferred code first includes the step of estimating a phase error based on a data sample from both a center of a data eye of input data and from a phase sample from the input data half-a-baud later in time. The phase error may be correlated with a sign of recovered data. The correlated phase error may be multiplied by a gain. The correlated and multiplied phase error may be filtered by a loop filter to generate an output. The output may be summed with a path output from at least one non-linear path. Most preferably there are three such non-linear paths. Finally, the summed output may be converted into clock phase information.

As illustratively depicted in Fig. 6, the aforementioned embodiments of the instant invention may be embodied in a receiver system. Preferably, the receiver system includes a receiver circuit **61** in electronic communication with an antenna **63**. Most preferably, a timing recovery system circuit **62** is also in electronic communication with the receiver circuit **61**. The timing recovery system circuit **62** is preferably in accordance with at least one of the embodiments described above. In preferred embodiments, the antenna **63** may receive an electronic signal and transmit this signal to the receiver circuit **61**. The receiver circuit may then further transmit an electronic signal to the timing recovery system circuit **62**.

While the description above refers to particular embodiments of the present invention, it will be understood that many modifications may be made without departing from the spirit thereof. The accompanying claims are intended to cover such modifications as would fall within the true scope and spirit of the present invention. The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims, rather than the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.